



Memory Expansion for the KIM

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Memory expansion for the KIM has already been discussed twice. The first time, in the November 1977 issue, it was shown how RAM could be added with the BEM-1 board, a kit for 2K of static RAM. The second time was in the July 1978 issue, when a board design for a 2K EPROM card was published, with the same bus connections as the BEM-1 card. This series now continues with a 4K static RAM board, also with the same bus. Connecting the RAM to the KIM requires address decoding and a bus buffer. A board has been designed for this as well.

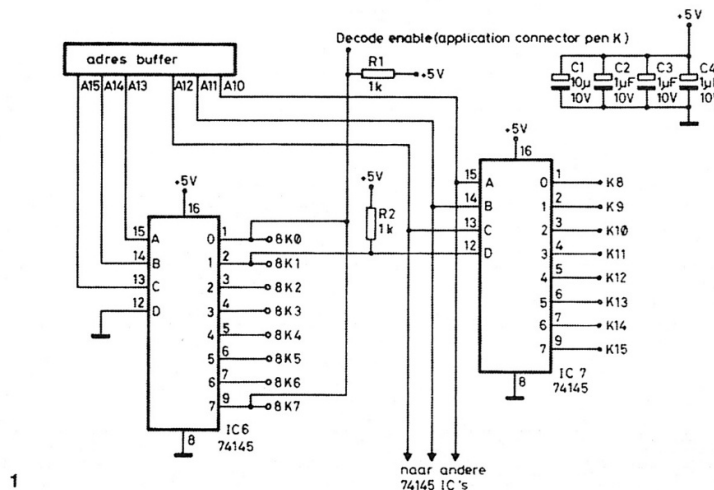


Fig. 1 Schematic diagram of the address decoding.

Address decoding

The 6502 microprocessor has 16 address output lines, A0-A15, which together form the address bus. With these, 64K of memory space can be addressed. The KIM does not use

address lines A13, A14 and A15, so only 8K of memory space is available. Of this, 4K is used on the KIM-1 board, which leaves 4K of memory space. The BEM-1 and the EPROM board were placed in this space.

The memory space of the KIM is divided into blocks of 1K byte. For each 1K there is a select line, starting with K0 up to K7. The way these select signals are generated is important, so we will look at it in more detail.

The select signals are generated by a 74LS145. This is a BCD-to-decimal decoder with four inputs A, B, C and D and 10 outputs 0 through 9. An output goes to zero when the number of that output matches the BCD number on the four inputs. In the KIM the D input is grounded via the connector (A-K, decode enable), and address lines A10, A11 and A12 are connected to the A, B and C inputs respectively. Only outputs 0 through 7 can now go low, depending on the address bus. These select lines divide the memory area of the KIM into 8 blocks of 1K. Output 0 is called K0, and so on up to K7.

This method of address selection means that in the KIM address 0000 is the same as address 2000 and address 4000, etc. Regardless of A13, A14 and A15, the 74LS145 decoder is always active.

Full memory expansion

To obtain a complete memory area, address lines A13, A14 and A15 must be included in the address selection. To do so, these address lines are connected to the A, B and C inputs respectively of a 74145 decoder (IC 6 in Fig. 1), and the D input is grounded. This gives us 8 address select lines, 8K0 to 8K7. Line 8K0 goes low when the microprocessor addresses 0000 to 1FFF, etc. The 8K lines thus divide the memory area into 8 blocks of 8K.

The KIM memory addresses are in the lowest 8K; select line 8K0 belongs to them. By connecting the D input of the 74LS145 KIM decoder (pin K of the application connector) to line 8K0 instead of to ground, the KIM memory locations can still be addressed. The higher addresses are now free, because for them line 8K0 is high.

1K select lines

Common memory ICs have 10 address line inputs and a CS (Chip Select) input. So a select signal for 1K must be connected to the CS input, because 10 address lines give 1024 possibilities. The 74LS145 KIM decoder provides the 1K select lines for the KIM memory area; these are K1 through K7. The KIM decoder is activated by the 8K0 signal. In exactly the same way (with 8K1 and address lines A10, A11 and A12), 1K select lines are generated by IC7, numbered consecutively K8 to K15. The 8K memory block 2000 to 3FFF is now divided into 8 blocks of 1K, selected by K8 to K15.

With another 74145 connected the same way, but now with the D input to 8K2, we get 1K select lines K16 through K23, memory area 4000 to 5FFF.

Continuing like this, we can divide the entire memory area into 64 blocks of 1K, numbered K0 through K63 (and not K65 as stated in the KIM manual!).

Vector selection

Very important memory addresses are those from which the interrupt vectors and the reset vector are fetched. On the 6502 these are located at the very top of the memory area, addresses FFFA to FFFF. On the KIM without the expansion described above, address FFFA is the same as address 1FFA. There is a ROM at that address, in which the vectors are fixed, as they should be.

If we now use the entire memory area, address 1FFA is no longer the same as FFFA, and the vector will be fetched from address FFFA etc. So the top of memory will have to contain a ROM holding the vectors. If we want to use the KIM monitor, the vectors will have to be exactly the same as the vectors at addresses 1FFA.

There is a simple trick that keeps the vectors in the KIM ROM while still allowing the memory to be expanded. The reason a 74145 was chosen as the decoder is that this IC has open-collector outputs, so outputs can be tied together. The trick is to tie select lines 8K0 and 8K7 together. Address space 0000 to 1FFF now coincides with address space E000 to FFFF, so the vectors at addresses 1FFA to 1FFF are fetched, once again from the KIM ROM. Lines 8K1 through 8K6 ensure that memory area 2000 to D000 is free.

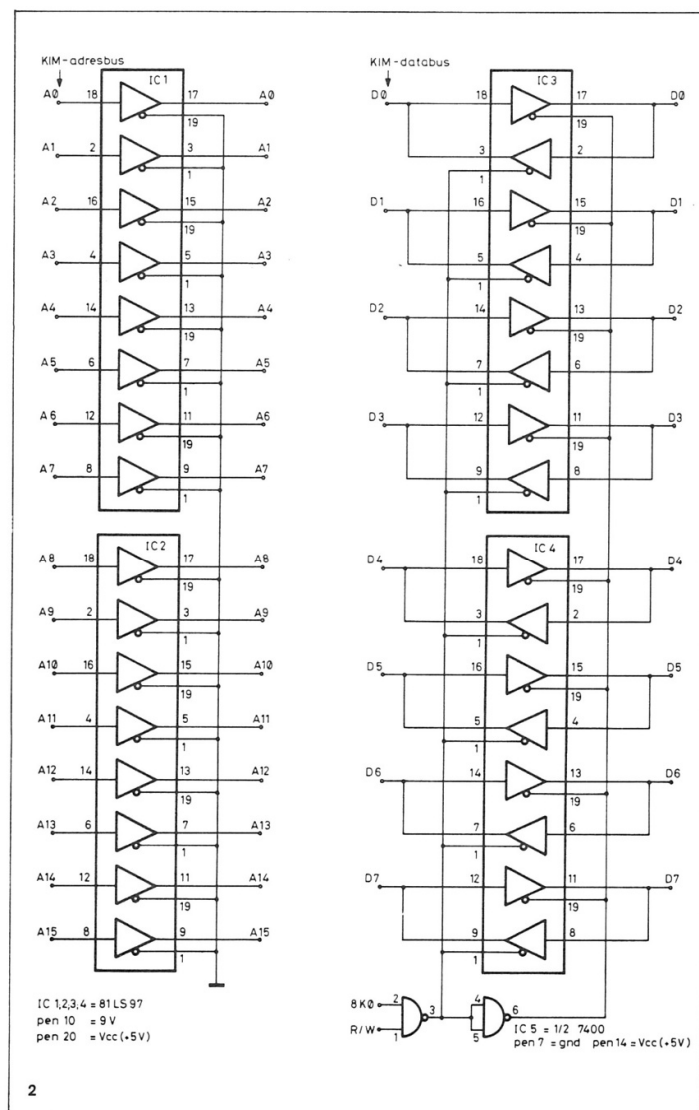
The result is that nothing changes for the KIM, except that memory is available from address 2000 upwards.

If 74145 ICs are used for all address decoders, we can place the vectors at the top of any 1K block x by connecting the corresponding Kx select line to 8K7. If 8K7 is also used for select lines K56 through K63, K64 takes over the role of 8K7. For the time being, 8K1 to 8K6 for memory expansion and the vectors from the KIM monitor will be enough for us, so 8K0 and 8K7 are linked on the board.

Bus buffer

The 6502 microprocessor is designed to work with TTL circuits. Even so, its outputs cannot be loaded too heavily; the 6502 data sheet states that an output can drive at most 1 TTL input and a capacitance of 130 pF. This applies to all outputs, including the data pins in the write state. Memory ICs such as the 2102 and 2114 are mostly MOS ICs with high-impedance inputs and negligible input currents. What is not negligible is the input capacitance, 10 pF per input on average. Long cables on the bus also form a considerable capacitive load. Buffering the address and data bus becomes necessary when more than 8K of memory is connected to the 6502.

Buffering the address bus is simple, because it is a one-way bus. Fig. 2 shows how all 16 address lines coming from the KIM board are buffered with two 81LS97s, each



containing 8 tri-state buffers. Because the tri-state control lines are tied permanently to ground, these buffers are always active. The data bus is not so easy to buffer, because it is a bidirectional bus. Data can be sent from the microprocessor to memory (write), but data transfer in the other direction is also possible (read). The direction of the data flow is indicated by the R/W signal. R/W is low during a write operation and high during a read operation. A data bus buffer must therefore also be bidirectional. This is possible by coupling two tri-state buffers: the input of one to the output of the other and vice versa (see Fig. 2). Only one of the tri-state buffers may then be activated, which is determined by the direction of the data flow. The data bus line is thus buffered for both directions. The control input of one tri-state buffer must be the inverse of the control input of the

other tri-state buffer. The control signal for the control inputs will be the R/W signal. The data bus buffering described above only works properly if the buffer is placed directly after the microprocessor. On the KIM this is not possible; the data bus goes unbuffered to the memory ICs on the KIM board. We will have to be content with buffering the data bus for the part of memory not reserved for the KIM, that is, for the memory area above address 2000. This means the buffer must not be activated in the direction of the microprocessor during a read operation from the KIM memory area. The select signal 8K0 is therefore also included in the control signals for the buffer, because 8K0 is low for addresses in the KIM memory area. This leads to the following:

During a read operation (R/W is high) from the KIM memory area (8K0 is low), the data buffer is activated away from the microprocessor.

During a read operation from the memory area above address 2000, the data buffer is activated towards the microprocessor. During a write operation (R/W is low), the data buffer is always activated away from the microprocessor.

In this way the data buffer can never try to drive the data bus at the same time as a memory on the KIM board.

We now have two data buses: an unbuffered data bus on the KIM board and a buffered data bus for the memory area above address 2000. For memory in the area 0300 to 13FF (K1 to K4), the unbuffered data bus will have to be used.

The link between 8K0 and 8K7 needed for vector selection means that the buffered data bus cannot be used for addresses E000 to FFFF either, because these coincide with addresses 0000 to 1FFF.

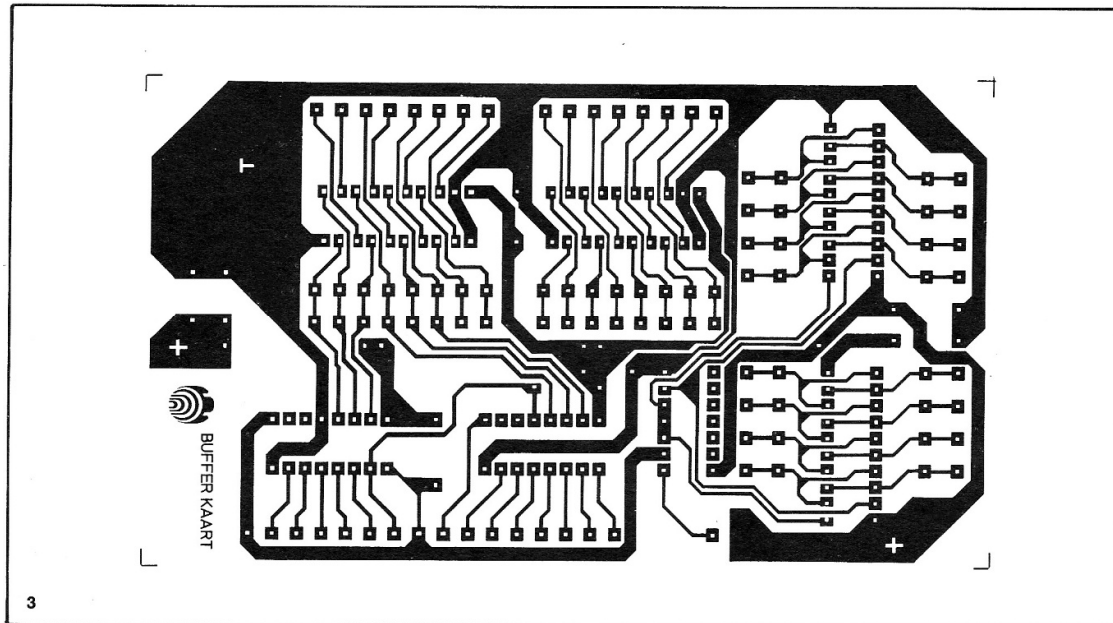


Fig. 3 Board layout of the board for the bus buffers and the address decoding circuit.

The board for address decoding and bus buffers

The circuits of Figs. 1 and 2 have been put together on one board. The board layout can be found in Fig. 3, the component layout in Fig. 4. Once the board has been populated and carefully checked, the address and data bus can be connected. In the component layout, the corresponding pins of the KIM expansion connector are shown next to the relevant connections. Do not forget to connect the R/W signal and decode enable (application connector K to 8K0). The wires between the KIM connector and the board must be kept as short as possible.

The unbuffered data bus is again available on the board for memory expansion in the area 0300 to 13FF. Power can easily be taken from the KIM power supply; the current consumption is about 100 mA maximum.

Correct operation of the board can be checked by running the KIM with the board connected. If all is well, the KIM works normally. When an address above 2000 is

selected, the KIM will show the page number of the memory address as data; for example, address 2000 gives 2000 20 on the KIM display.

4K RAM memory

We now have the option of adding a lot of memory; a board with a lot of memory that takes up little space is a good addition.

A memory IC that is rapidly falling in price is the 2114, a 1K x 4 bit static RAM. Only two 2114s are needed for 1K byte of RAM. On a Eurocard-size board (10 x 16 cm) we can easily fit 8 2114 ICs, 4K bytes of RAM in total.

On the 2114 the data inputs and outputs are combined, which keeps the number of pins down to 18 and means no tri-state buffers are needed, as with the 2102 ICs on the BEM-1 board. The 2114 pinout is shown in Fig. 5, the schematic of the 4K RAM board in Fig. 6. The circuit is very simple: just a set of 2114 ICs, pull-up resistors for the chip select lines (called S1, S2, S3 and S4, consistent with the other memory boards) and a number of decoupling capacitors.

The 4K RAM board is single-sided; a number of wire links were unavoidable. This drawback does not outweigh the cost of a double-sided board. The component layout is shown in Fig. 7. The ICs are best mounted in IC sockets; replacing a faulty IC is then much easier.

The board connector

The 4K RAM board is fitted with a 31-pin (DIN 41617) connector, the same as on the BEM-1 and the EPROM board. The connections are also in the same positions on the connector. Because the board carries 4K of RAM, two additional select lines (S3, S4) must be brought in. Two previously unused connector pins are used for this (16 = S3, 14 = S4).

The connector pinout including this extension is given in Table 1.

This makes the BEM-1, the EPROM board and the 4K RAM board fully interchangeable. Instead of a BEM-1 board, a 4K RAM board can be used with, for example, only IC1 through IC4 fitted; the 4K RAM board is then reduced to 2K RAM.

The 4K RAM board can be placed in the KIM memory area 0300 to 13FF, which is then completely full. In combination with the bus buffer and address decoding board, expansion by 16K, up to a maximum of 24K RAM, is no problem. Even more memory will again require bus buffers.

Powering the 4K RAM board

According to the specifications, a 2114 IC draws a maximum supply current of 100 mA. There is a low-power version, the 2114L, with a maximum current consumption of 65 mA. With 2114 ICs the whole board will draw 0.8 A. Measurements on two 4K RAM boards showed an average current consumption of 0.4 A. So two 4K RAM boards can be connected to a 1 A / 5 V supply, which can be built with a 7805 regulator.

Using other memory boards

Perhaps you are already using extra memory; there are, for example, various 8K RAM cards on the market, such as the Memory Plus card. These memory cards usually have address decoding circuitry on the board itself. Where the RAM sits in the memory map can be set with switches on the board. Supplying the select lines is then not necessary. Buffering the data and address bus is still recommended, however. The bus buffer board is well suited for this too. It is connected to the KIM-1 in the same way as described above. Only IC7, which generates the 1K select signals, can be omitted. The 'decode enable' signal does come from the bus buffer board and not from the memory card. A bus buffer board can take 24K of RAM or ROM without further ado, in the form of the 4K RAM board described here, the EPROM board, the BEM-1 or other memory cards without data buffers, such as the Memory Plus card.

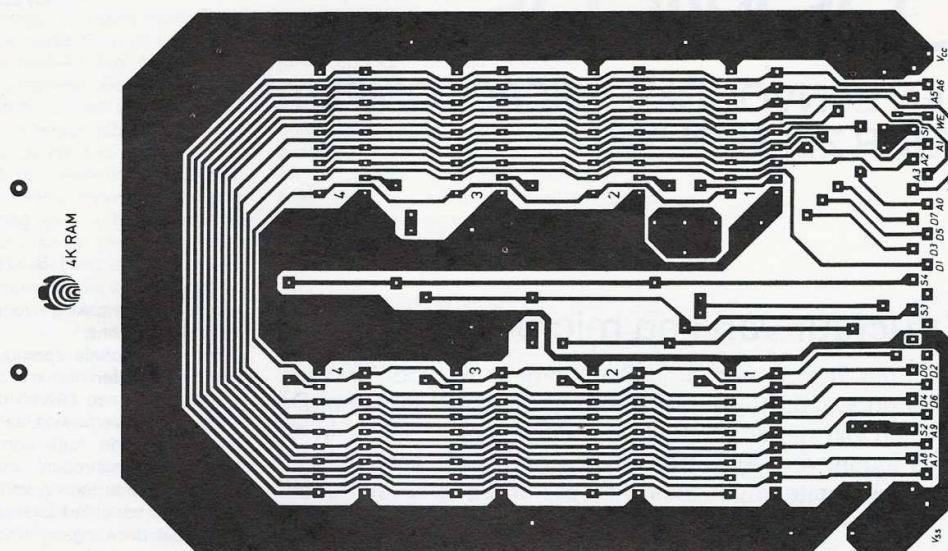
Tabel 1 De aansluitingen van de 31-polige connector volgens DIN 41617.

Pen	Functie
1	GND
2	GND
3	A7
4	A8
5	A9
6	S2
7	D6
8	D4
9	D2
10	D0
11	NC
12 -	5 V
13	+12 V
14	S4
15	R/W
16	S3
17	D1
18	D3
19	D5
20	D7
21	A0
22	A4
23	A3
24	A2
25	A1
26	S1
27	RAM R/W
28	A5
29	A6
30	+5V
31	+5 V

Fig. 4 Component layout of the board for the bus buffers and the address decoding circuit. Fig. 5 Pinout of the 2114 memory IC.



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afb. 7 Printontwerp van de 4K-RAM print
afb. 8 Componentenopstelling van de 4K
RAM-print.

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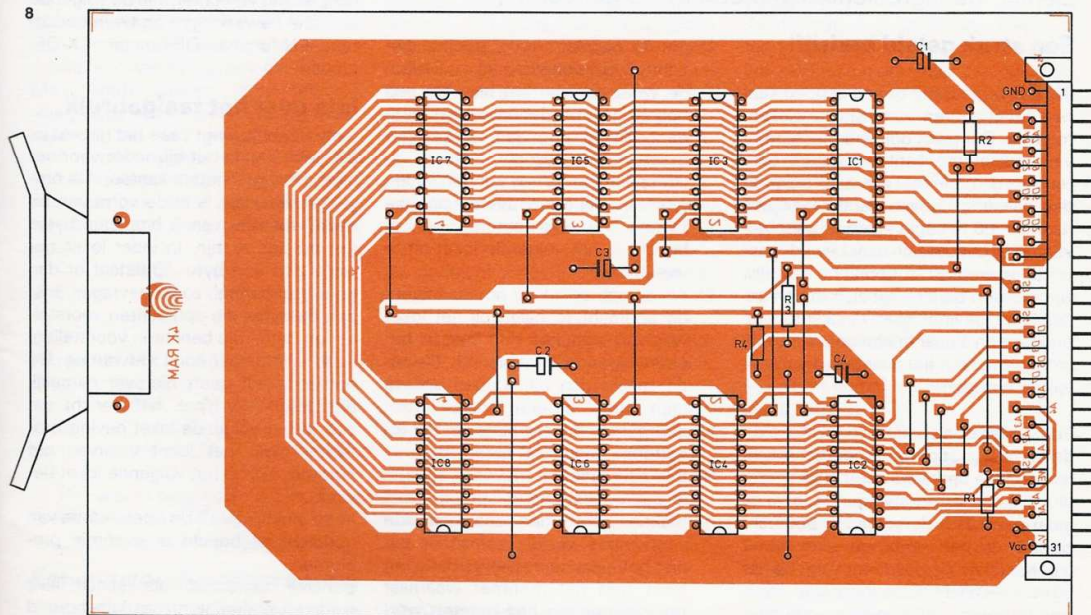


Fig. 6 Schematic diagram of the 4K RAM board.